GUJARAT TECHNOLOGICAL UNIVERSITY

(Established Under Gujarat Act. No.:20 of 2007)

Date: 22-05-2017

CIRCULAR

Interested faculty members and students may register for the following webinar which is going to be held on Thu, May 25, 2017 3:30 PM - 4:30 PM IST.

Virtual Academy: "Design and Verification of Digital Systems on FPGA"

Thu, May 25, 2017 3:30 PM - 4:30 PM IST

Registration URL: https://attendee.gotowebinar.com/register/6707654630010492417

Description:

In recent days, design of digital systems for real time applications has become very significant in order to achieve optimum performance. So, this webinar demonstrates the insight techniques adopted for design of digital systems on Field Programmable Gate Array (FPGA) devices.

The objectives of the webinar are as follows.

1. Introduction to Digital System Design and FPGA devices.
2. Abstraction levels of Digital System Design.
3. Digital Systems Behavior Verification methods.
4. Xilinx tool flow for Design of Digital Systems on FPGA Devices.
5. Variants of Xilinx FPGA Device.

Presenter:

Dr. Mahendra V,
Professor, MLR Institute of Technology,
Hyderabad.

Sd/-
Registrar (I/c)